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Description

MOTOR CONTROL CIRCUIT FOR SUPPLYING A CONTROLLABLE DRIVING VOLTAGE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a motor control circuit and, more particularly, to a motor control circuit for supplying a controlling driving voltage to a motor.

[0003] 2. Description of the Related Art

[0004] Generally speaking, an H-bridge circuit constructed by four switch transistors may supply a driving voltage to a motor, such as DC motor, stepping motor, voice coil motor, and the like, for controlling a rotating direction, a rate of rotation, and other operational characteristics.

[0005] FIG. 1 is a circuit diagram showing a conventional H-bridge circuit 10 for driving a motor M. Referring to FIG. 1, the motor M is coupled between a supply voltage

source V_m and a ground potential through the H-bridge circuit 10. Although the motor M is in practice a complex system consisting of a variety of mechanical and electrical components, the driving voltage is essentially applied to a winding of the motor M for generating a magnetic field. Consequently, the term "motor" in this specification primarily refers to the winding of the motor M, which may be reduced to an inductive load for a simpler consideration. The drawing also emphasizes this consideration by illustrating the representative winding of the motor M.

[0006] The H-bridge circuit 10 includes four N-channel MOSFET transistors (NMOS) Q_1 to Q_4. The NMOS transistor Q_1 has a drain electrode coupled to the supply voltage source V_m and a source electrode coupled to a terminal A of the motor M. The NMOS transistor Q_2 has a drain electrode coupled to the supply voltage source V_m and a source electrode coupled to a terminal B of the motor M. The NMOS transistor Q_3 has a drain electrode coupled to the terminal A of the motor A and a source electrode coupled to a ground potential. The NMOS transistor Q_4 has a drain electrode coupled to the terminal B of the motor M and a source electrode coupled to the ground potential.

[0007] Since the NMOS transistors Q_1 to Q_4 have parasitic diodes

D_1 to D_4, respectively, the H-bridge circuit 10 needs not to be additionally provided with flywheel diodes. If the four switch transistors of the H-bridge circuit 10 are implemented by bipolar junction transistors, however; the diodes D_1 to D_4 shown in FIG. 1 should be additionally provided.

[0008] The gate electrodes of the NMOS transistors Q_1 to Q_4 are controlled by control signals G_1 to G_4, respectively. When the control signals G_1 and G_4 are at a logic high level and the control signals G_2 and G_3 are at a logic low level, the NMOS transistors Q_1 and Q_4 are turned on and the NMOS transistors Q_2 and Q_3 are turned off such that the terminal A is coupled to the supply voltage source V_m through the conductive NMOS transistor Q_1 and the terminal B is coupled to the ground potential through the conductive NMOS transistor Q_4. As a result, the supply voltage source V_m applies a driving voltage to the motor M, causing a driving current I_1 to flow through the motor M in a direction from the terminal A toward the terminal B. When the control signals G_1 and G_4 are at the logic low level and the control signals G_2 and G_3 are at the logic high level, the NMOS transistors Q_1 and Q_4 are turned off and the transistor Q_2 and Q_3 are turned on such that the terminal B is

coupled to the supply voltage source V_m through the conductive NMOS transistor Q_2 and the terminal A is coupled to the ground potential through the conductive NMOS transistor Q_3. As a result, the supply voltage source V_m applies another driving voltage to the motor M, causing another driving current I_2 to flow through the motor M in another direction from the terminal B toward the terminal A.

[0009] Among the various applications of using the motor M, the driving voltage applied between the terminals A and B determines practical operational characteristics of the motor M and therefore needs to satisfy several requirements of application. At first, a polarity and an absolute value of the driving voltage should belong to a controllable quantity because the polarity of the driving voltage determines a direction of the magnetic field generated by the winding of the motor M and the absolute value of the driving voltage determines a strength of the magnetic field generated by the motor M. Especially when the motor M needs to be operated in a constant voltage driving condition, the absolute value of the driving voltage must be kept constant.

[0010] Conventionally, a pulse width modulation (PWM) technique is usually adopted to control the absolute value of the

driving voltage applied to the motor. More specifically, in the situation where the NMOS transistor Q_4 is turned on and the NMOS transistors Q_2 and Q_3 are turned off, the control signal G_1 may be implemented by a PWM signal such that the ON time of the NMOS transistor Q_1 is determined by the duty cycle of the PWM control signal G_1, thereby controlling an average value of the driving voltage. However, the PWM technique inevitably induces excessive disturbances in the supply voltage source V_m and the driving voltage applied to the motor M. For the application which requires extremely precise control of the motor, the conventional PWM technique may cause several disadvantageous effects. Therefore, it is desired to provide a control circuit capable of supplying a low noise driving voltage to the motor M.

SUMMARY OF INVENTION

[0011] An object of the present invention is to provide a motor control circuit capable of controlling a polarity and an absolute value of the driving voltage for a motor.

[0012] Another object of the present invention is to provide a motor control circuit capable of keeping constant an absolute value of a driving voltage for a motor.

[0013] Still another object of the present invention is to provide a

motor control circuit capable of suppressing noise of a driving voltage for a motor.

[0014] According to the present invention, a motor control circuit is provided for supplying a driving voltage to a motor. The driving voltage is applied between a first terminal and a second terminal of the motor. The motor control circuit includes: an H-bridge circuit, a voltage detection circuit, an error amplifier, a feedback circuit, and a state control circuit.

[0015] The H-bridge circuit has a first linear unit, a second linear unit, a first switching unit, and a second switching unit. The first linear unit and the first switching unit are together coupled to the first terminal. The second linear unit and the second switching unit are together coupled to the second terminal. The voltage detection circuit generates at least one voltage detection signal representative of the driving voltage of the motor. The error amplifier generates at least one error signal representative of a difference between the at least one voltage detection signal and a command voltage signal. The at least one error signal is electrically separate from the first and the second switching units. The feedback circuit is coupled to the error amplifier for receiving the at least one error signal so

as to apply the at least one error signal selectively to the first or the second linear unit. The state control circuit synchronously controls the first and the second switching units and the feedback circuit.

[0016] During a first operational period, the first switching unit is operated in a nonconductive mode, the second switching unit is operated in a conductive mode, the feedback circuit allows one of the at least one error signal to be applied to the first linear unit for operating the first linear unit in a linear mode, and the feedback circuit prevents the at least one error signal from being applied to the second linear unit. Therefore, the driving voltage is controlled to become substantially proportional to the command voltage signal. At this moment, the driving voltage causes a current to flow through the motor in a direction from the first terminal toward the second terminal.

[0017] During a second operational period, the first switching unit is operated in the conductive mode, the second switching unit is operated in the nonconductive mode, the feedback circuit prevents the at least one error signal from being applied to the first linear unit, and the feedback circuit allows another of the at least one error signal to be applied to the second linear unit for operating the

second linear unit in the linear mode. Therefore, the driving voltage is controlled to become substantially proportional to the command voltage signal. At this moment, the driving voltage causes a current to flow through the motor in a direction from the second terminal toward the first terminal.

[0018] The voltage detection circuit includes a first voltage divider and a second voltage divider. The first voltage divider is coupled between the first terminal and a ground potential, for outputting a first terminal division voltage signal as the one of the at least one voltage detection signal. The second voltage divider is coupled between the second terminal and the ground potential, for outputting a second terminal division voltage signal as the another of the at least one voltage detection signal.

[0019] The error amplifier includes a first, a second, and a third NMOS transistors, and a first, a second, and a third current mirrors. The first NMOS transistor has a gate electrode controlled by the first terminal division voltage and a source electrode coupled to a constant current source. The second NMOS transistor has a gate electrode controlled by the second terminal division signal and a source electrode coupled to the constant current source. The

third NMOS transistor has a gate electrode controlled by the command voltage signal and a source electrode coupled to the constant current source. The first current mirror has an original current branch coupled to a drain electrode of the first NMOS transistor and a drain electrode of the second NMOS transistor. The second current mirror has an original current branch coupled to a drain electrode of the third NMOS transistor. The third current mirror has an original current branch coupled to a mirror current branch of the first current mirror. A first output terminal is coupled to a mirror current branch of the second current mirror and a mirror current branch of the third current mirror, for supplying the one of the at least one error signal.

[0020] The second current mirror further has a parallel mirror current branch coupled in parallel with the mirror current branch of the second current mirror. The third current mirror further has a parallel mirror current branch coupled in parallel with the mirror current branch of the third current mirror. The error amplifier further includes a second output terminal coupled to the parallel mirror current branch of the second current mirror and the parallel mirror current branch of the third current mirror, for supply-

ing the another of the at least one error signal.

[0021] The feedback circuit includes a first and a second switching means. The first switching means is coupled to the first linear unit and controlled by the state control circuit. During the first operational period, the first switching means allows the one of the at least one error signal to be applied to the first linear unit. During the second operational period, the first switching means prevents the at least one error signal from being applied to the first linear unit. The second switching means is coupled to the second linear unit and controlled by the state control circuit. During the first operational period, the second switching means prevents the at least one error signal from being applied to the second linear unit. During the second operational period, the second switching means allows the another of the at least one error signal to be applied to the second linear unit.

[0022] The state control circuit synchronously outputs a first to a fourth state control signals, for controlling the first and the second switching means of the feedback circuit and the first and the second switching units of the H-bridge circuit, respectively. Each of the first to the fourth state control signals is a digital logic signal having a logic high

level and a logic low level. During the first operational period, the first and the third state control signals are at the logic low level and the second and the fourth state control signals are at the logic high level. During the second operational period, the first and the third state control signals are at the logic high level and the second and the fourth state control signals are at the logic low level.

[0023] The motor control circuit further includes a brake circuit controlled by the state control circuit. During a third operational period, the brake circuit transforms the at least one error signal to become at least one brake signal. The at least one brake signal is applied through the feedback circuit simultaneously to the first and the second linear units for operating the first and the second linear units in the linear mode. During the third operational period, the state control circuit operates the first and the second switching units in the nonconductive mode.

[0024] The state control circuit further outputs a brake control signal, which is a digital logic signal having a logic high level and a logic low level. The brake control signal is outputted to the brake circuit for transforming the at least one error signal to become the at least one brake signal. During the third operational period, the first to the fourth

state control signals are at the logic low level and the brake control signal is at the logic high level.

BRIEF DESCRIPTION OF DRAWINGS

[0025] The above-mentioned and other objects, features, and advantages of the present invention will become apparent with reference to the following descriptions and accompanying drawings, wherein:

[0026] FIG. 1 is a circuit diagram showing a conventional H-bridge circuit for driving a motor;

[0027] FIG. 2 is a circuit diagram showing an example of a motor control circuit according to the present invention;

[0028] FIG. 3 is a detailed circuit diagram showing an example of an error amplifier and a brake circuit according to the present invention; and

[0029] FIG. 4 is a timing chart showing three operational states of a motor control circuit according to the present invention.

DETAILED DESCRIPTION

[0030] The preferred embodiments according to the present invention will be described in detail with reference to the drawings.

[0031] FIG. 2 is a circuit diagram showing an example of a motor control circuit 20 according to the present invention. Re-

ferring to FIG. 2, the motor control circuit 20 includes an H-bridge circuit 21, a voltage detection circuit 22, an error amplifier 23, a feedback circuit 24, and a state control circuit 25.

[0032] The H-bridge circuit 21 includes two linear units LQ_1 and LQ_2 and two switching units SQ_1 and SQ_2. The linear units LQ_1 and LQ_2 couple a supply voltage source V_m and a motor M while the switching units SQ_1 and SQ_2 couples the motor M and a ground potential. The linear units LQ_1 and LQ_2 may be operated in a linear mode, a conductive mode, and a nonconductive mode while the switching units SQ_1 and SQ_2 may be operated in the conductive mode and the nonconductive mode. The term "linear mode" refers to an operational state in which an equivalent resistance substantially linearly changes in accordance with a control signal. The term "conductive mode" refers to an operational state in which the equivalent resistance is negligible and therefore considered as a short circuit. The term "nonconductive mode" refers to an operational state in which the equivalent resistance is large enough for being considered as an open circuit.

[0033] The voltage detection circuit 22 is adopted to detect a driving voltage for the motor M, i.e. a voltage applied be-

tween terminals A and B of the motor M, and then output to the inverting input terminal (-) of the error amplifier 23 at least one voltage detection signal V_d representative of the motor driving voltage. The non-inverting input terminal (+) of the error amplifier 23 receives a command voltage signal V_{com} for instructing the motor control circuit 20 according to the present invention to generate a desirable motor driving voltage. The command voltage signal V_{com} may be set by users, adjusted according to application requirements, or controlled by other circuit components based on the feedback of operational characteristics of the motor. In the error amplifier 23, the at least one voltage detection signal V_d is compared with the command voltage signal V_{com}, generating at least one error signal V_e representative of a difference between the at least one voltage detection signal V_d and the command voltage signal V_{com}.

[0034] Based on state control signals S_1 and S_2 generated by the state control circuit 25, the feedback circuit 24 causes the at least one error signal V_e to be selectively applied to the linear unit LQ_1 or LQ_2. More specifically, when the state control signals S_1 and S_2 instructs the feedback circuit 24 that the linear unit LQ_1 is to be operated in the linear

mode and the linear unit LQ_2 is to be operated in the non-conductive mode, the feedback circuit 24 allows the at least one error signal V_e to be applied to the linear unit LQ_1 but prevents the at least one error signal V_e from being applied to the linear unit LQ_2. In this case, the equivalent resistance of the linear unit LQ_1 substantially linearly changes in accordance with the at least one error signal V_e. When the state control signals S_1 and S_2 instructs the feedback circuit 24 that the linear LQ_1 is to be operated in the nonconductive mode and the linear unit LQ_2 to be operated in the linear mode, the feedback circuit 24 prevents the at least one error signal V_e from being applied to the linear unit LQ_1 but allows the at least one error signal V_e to be applied to the linear unit LQ_2. In this case, the equivalent resistance of the linear unit LQ_2 substantially linearly changes in accordance with the at least one error signal V_e.

[0035] The state control circuit 25 further generates other two state control signals S_3 and S_4 for controlling the switching units SQ_1 and SQ_2 to be operated in either the conductive mode or the nonconductive mode. The state control signals S1 to S4 synchronously generated by the state control circuit 25 are collaborative with respect to each

other, thereby achieving the operational state control performed in the motor control circuit 20 according to the present invention.

[0036] More specifically, when the state control signal S_1 causes the feedback circuit 24 to selectively applies the at least one error signal V_e to the linear unit LQ_1, the state control signal S_4 operates the switching unit SQ_2 in the conductive mode. At this moment, the state control signals S_2 and S_3 operate the linear unit LQ_2 and the switching unit SQ_1 in the nonconductive mode, respectively. As a result, the terminal A of the motor M is coupled to the supply voltage source V_m though the linear unit LQ_1 operated in the linear mode while the terminal B of the motor M is connected in short circuit to the ground potential. Since the terminal B is at a substantially zero voltage, the voltage of the terminal A indicates the motor driving voltage. In this case, the driving current flows through the motor M in a direction from the terminal A toward the terminal B. As described above, the variation of the motor driving voltage is fed back to the linear unit LQ_1 through a loop constructed by the voltage detection circuit 22, the error amplifier 23, and the feedback circuit 24, causing the equivalent resistance of the linear unit LQ_1 to correspondingly

change for controlling the motor driving voltage to become substantially proportional to the command voltage signal V_{com}.

[0037] On the other hand, when the state control signal S_2 causes the feedback circuit 24 to selectively apply the at least one error signal V_e to the linear unit LQ_2, the state control signal S_3 operates the switching unit SQ_1 in the conductive mode. At this moment, the state control signals S_1 and S_4 operate the linear unit LQ_1 and the switching unit SQ_2 in the nonconductive mode, respectively. As a result, the terminal B of the motor M is coupled to the supply voltage source V_m though the linear unit LQ_2 operated in the linear mode while the terminal A of the motor M is connected in short circuit to the ground potential. Since the terminal A is at a substantially zero voltage, the voltage of the terminal B indicates the motor driving voltage. In this case, the driving current flows through the motor M in a direction from the terminal B toward the terminal A. As described above, the variation of the motor driving voltage is fed back to the linear unit LQ_2 through a loop constructed by the voltage detection circuit 22, the error amplifier 23, and the feedback circuit 24, causing the equivalent resistance of the linear unit LQ_2 to correspondingly

change for controlling the motor driving voltage to become substantially proportional to the command voltage signal V_{com}.

[0038] Therefore, the motor control circuit 20 according to the present invention is able to control the polarity and absolute value of the driving voltage for the motor. If the command voltage signal V_{com} is set as a constant, the motor control circuit 20 according to the present invention is able to keep constant the absolute value of the driving voltage for the motor. Because the motor control circuit 20 according to the present invention utilizes the linear modes of the linear units LQ_1 and LQ_2 to achieve the desired motor driving voltage, the noise of the driving voltage is effectively suppressed.

[0039] It should be noted that in the motor control circuit 20 according to the present invention, the switching units SQ_1 and SQ_2 are controlled by the state control signals S_3 and S_4 generated by the state control circuit 25, instead of the at least one error signal V_e. Particularly, the at least one error signal V_e is electrically separate from the switching units SQ_1 and SQ_2. As a primary function, the at least one error signal V_e is selectively fed back to operate the linear unit LQ_1 or LQ_2 in the linear mode.

[0040] In the embodiment shown in FIG. 2, the linear units LQ_1 and LQ_2 may be implemented by NMOS transistors. The linear unit LQ_1 has a drain electrode coupled to the supply voltage source V_m and a source electrode coupled to the terminal A of the motor M. The linear unit LQ_2 has a drain electrode coupled to the supply voltage source V_m and a source electrode coupled to the terminal B of the motor M. The switching units SQ_1 and SQ_2 may be implemented by NMOS transistors. The switching unit SQ_1 has a drain electrode coupled to the terminal A of the motor M and a source electrode coupled to the ground potential. The switching unit SQ_2 has a drain electrode coupled to the terminal B of the motor M and a source electrode coupled to the ground potential.

[0041] It should be noted that the H-bridge circuit 21 shown in FIG. 2 needs not to be additionally provided with flywheel diodes since the NMOS transistors have parasitic diodes D_1 to D_4. If the linear units LQ_1 and LQ_2 and the switching units SQ_1 and SQ_2 of the H-bridge circuit 21 are implemented by bipolar junction transistors, however; the diodes D_1 to D_4 shown in FIG. 2 must be additionally provided.

[0042] The voltage detection circuit 22 may be constructed by

two voltage dividers 22_1 and 22_2 for detecting the voltages at the terminals A and B of the motor M, respectively. The voltage divider 22_1 is implemented by resistors R_1 and R_3 series-connected between the terminal A and the ground potential. The voltage detection signal V_{d1} is asserted at the coupled point of the resistors R_1 and R_3, having a ratio of $R_3/(R_1+R_3)$ with respect to the voltage at the terminal A. The voltage divider 22_2 is implemented by resistors R_2 and R_4 series-connected between the terminal B and the ground potential. The voltage detection signal V_{d2} is asserted at the coupled point of the resistors R_2 and R_4, having a ratio of $R_4/(R_2+R_4)$ with respect to the voltage at the terminal B. The resistors R_1 to R_4 may be designed to satisfy a condition that $R_3/(R_1+R_3)$ is equal to $R_4/(R_2+R_4)$. In the embodiment shown in FIG. 2, the at least one voltage detection signal V_d consists of the voltage detection signals V_{d1} and V_{d2}, representative of the motor driving voltage.

[0043] It should be noted that although in the embodiment shown in FIG. 2 the voltage detection circuit 22 outputs two voltage detection signals V_{d1} and V_{d2}, the present invention is not limited to this and may be applied to a case that the voltage detection circuit 22 further includes an

analog comparator for obtaining a difference between the voltages of the terminals A and B to generate a single voltage detection signal V_d representative of the motor driving voltage.

[0044] The error amplifier 23 has two inverting input terminals for receiving the voltage detection signals V_{d1} and V_{d2}, respectively. As described above, when the motor M is operated in the condition that the driving current flows from the terminal A toward the terminal B, the motor driving voltage is substantially equal to the voltage at the terminal A and the terminal B is connected in short circuit to the ground potential, so the voltage detection signal V_{d1} is representative of the motor driving voltage and the voltage detection signal V_{d2} is substantially zero. As a result, the error amplifier 23 compares in effect the voltage detection signal V_{d1} and the command voltage signal V_{com}. On the other hand, when the motor M is operated in the condition that the driving current flows from the terminal B toward the terminal A, the motor driving voltage is substantially equal to the voltage at the terminal B and the terminal A is connected in short circuit to the ground potential, so the voltage detection signal V_{d2} is representative of the motor driving voltage and the voltage detection

signal V_{d1} is substantially zero. As a result, the error amplifier 23 compares in effect the voltage detection signal V_{d2} and the command voltage signal V_{com}.

[0045] The error amplifier 23 has two identical output terminals O_1 and O_2 for generating two identical error signals V_{e1} and V_{e2} as the at least one error signal V_e. The output terminal O_1 is coupled to the linear unit LQ_1 while the output terminal O_2 is coupled to the linear unit LQ_2. The feedback circuit 24 is provided with two switching means SW_1 and SW_2. The switching means SW_1 is controlled by the state control signal S_1. When the switching means SW_1 is turned on, the output terminal O_1 is connected in short circuit to the ground potential, preventing the error signal V_{e1} from being applied to the linear unit LQ_1 and causing the linear unit LQ_1 to be operated in the nonconductive mode. When the switching means SW_1 is turned off, the error signal V_{e1} is applied to the linear unit LQ_1 for operating the linear unit LQ_1 in the linear mode. The switching means SW_2 is controlled by the state control signal S_2. When the switching means SW_2 is turned on, the output terminal O_2 is connected in short circuit to the ground potential, preventing the error signal V_{e2} from being applied to the linear unit LQ_2 and causing the linear unit LQ_2

to be operated in the nonconductive mode. When the switching means SW_2 is turned off, the error signal V_{e2} is applied to the linear unit LQ_2 for operating the linear unit LQ_2 in the linear mode.

[0046] It should be noted that although in the embodiment shown in FIG. 2 the feedback circuit 24, under the control of the state control circuit 25, independently determines whether the error signal V_{e1} is applied to or not to the linear unit LQ_1 and independently determines whether the error signal V_{e2} is applied to or not to the linear unit LQ_2, the present invention is not limited to this and may be applied to a case that the error amplifier 23 is provided with only one output terminal for generating a single error signal V_e. In this case, the feedback circuit 24 under the control of the state control circuit 25 causes the single output terminal of the error amplifier 23 to be selectively coupled to the linear unit LQ_1 or LQ_2, thereby achieve selectively applying the single error signal V_e to the linear unit LQ_1 or LQ_2.

[0047] Since the linear units LQ_1 and LQ_2 of the H-bridge circuit 21 are operated in the linear mode, instead of being switched on and off with a high frequency according to the prior art PWM technique, the motor control circuit 20

according to the present invention avoids the induction of excessive disturbances and therefore effectively suppresses the noise of the motor driving voltage. If a greater degree of suppression to the noise of the motor driving voltage is desired, the feedback circuit 24 may further be provided with capacitors C_1 and C_2. The capacitor C_1 is coupled between the gate electrode of the linear unit LQ_1 and the ground potential such that the error signal V_{e1} is relatively gradually applied to the gate electrode of the linear unit LQ_1. The capacitor C_2 is coupled between the gate electrode of the linear unit LQ_2 and the ground potential such that the error signal V_{e2} is relatively gradually applied to the gate electrode of the linear unit LQ_2.

[0048] The motor control circuit 20 according to the present invention is further provided with a brake circuit 26 for simultaneously operating the linear units LQ_1 and LQ_2 in the conductive mode. More specifically, when the motor control circuit 20 performs the brake control, the state control circuit 25 outputs a brake control signal BRK to the brake circuit 26. In response to the brake control signal BRK, the brake circuit 26 transforms the at least one error signal V_e generated by the error amplifier 23 to become at least one brake signal. Under the control of the state con-

trol circuit 25, the switching units SQ_1 and SQ_2 are operated in the nonconductive mode, and the feedback circuit 24 simultaneously applies the at least one brake signal to the linear units LQ_1 and LQ_2 for operating the linear units LQ_1 and LQ_2 in the conductive mode.

[0049] More specifically, in the embodiment shown in FIG. 2, the brake circuit 26 in response to the brake control signal BRK causes the two inverting input terminals of the error amplifier 23 to be connected in short circuit to the ground potential or held at a potential lower than the command voltage signal V_{com}. As a result, the error signals V_{e1} and V_{e2} are transformed to become the brake signals having the logic high level, not any more the above-described linear signals for the feedback control. In this case, the state control circuit 25 simultaneously turns off the switching means SW_1 and SW_2 through the state control signals S_1 and S_2 such that the brake signals V_{e1} and V_{e2} having the logic high level are input to the gate electrodes of the linear units LQ_1 and LQ_2, respectively. The brake signals V_{e1} and V_{e2} having the logic high level operate the linear units LQ_1 and LQ_2 in the conductive mode, achieving the desired brake control.

[0050] In the brake control, for more rapidly transforming the er-

ror signals V_{e1} and V_{e2} to become the brake signals having the logic high level, the brake circuit 26 may be additionally provided with means for directly controlling the output stages of the error amplifier 23 so as to force the two output terminals O_1 and O_2 to rapidly output the brake signals V_{e1} and V_{e2} having the logic high level.

[0051] FIG. 3 is a detailed circuit diagram showing an example of the error amplifier 23 and the brake circuit 26 according to the present invention. First of all is described the detailed circuit of one example of the error amplifier 23 according to the present invention. An NMOS transistor N_1 has a gate electrode for receiving the voltage detection signal V_{d1}, an NMOS transistor N_2 has a gate electrode for receiving the voltage detection signal V_{d2}, and an NMOS transistor N_3 has a gate electrode for receiving the command voltage signal V_{com}. Each of the NMOS transistors N_1 to N_3 has a source electrode coupled to a constant current source I_{ea}. When the voltage detection signal V_{d2} is zero, the NMOS transistor N_2 is turned off. In this case, the voltage detection signal V_{d1} and the command voltage signal V_{com} determines a ratio of the current flowing through the NMOS transistors N_1 to the current flowing through the NMOS transistor N_3, on which a differential

distribution of the constant current source I_{ea} depends. When the voltage detection signal V_{d1} is zero, the NMOS transistor N_1 is turned off. In this case, the voltage detection signal V_{d2} and the command voltage signal V_{com} determines a ratio of the current flowing through the NMOS transistors N_2 to the current flowing through the NMOS transistor N_3, on which a differential distribution of the constant current source I_{ea} depends.

[0052] PMOS transistors P_1 and P_3 form a current mirror in which the PMOS transistor P_1 serves as an original current branch and the PMOS transistor P_3 serves as a mirror current branch. The PMOS transistor P_1 is coupled to the NMOS transistors N_1 and N_2 such that the current flowing through the PMOS transistor P_3 corresponds in accordance with the mirror effect to the current flowing through the NMOS transistor N_1 (or N_2), for being representative of the voltage detection signal V_{d1} (or V_{d2}). PMOS transistors P_2 and P_4 form another current mirror in which the PMOS transistor P_2 serves as an original current branch and the PMOS transistor P_4 serves as a mirror current branch. The PMOS transistor P_2 is coupled to the NMOS transistor N_3 such that the current flowing through the PMOS transistor P_4 corresponds in accordance with the mirror effect to the

current flowing through the NMOS transistor N_3, for being representative of the command voltage signal V_{com}.

[0053] NMOS transistors N_4 and N_5 form still another current mirror in which the NMOS transistor N_4 serves as an original current branch and the NMOS transistor N_5 serves as a mirror current branch. The NMOS transistor N_4 is coupled to the PMOS transistor P_3 such that the current flowing through the NMOS transistor N_5 corresponds in accordance with the mirror effect to the current flowing through the NMOS transistor N_1 (or N_2), for being representative of the voltage detection signal V_{d1} (or V_{d2}).

[0054] The output terminal O_1 of the error amplifier 23 is coupled to the PMOS transistor P_4 and the NMOS transistor N_5. When the voltage detection signal V_{d1} (or V_{d2}) is lower than the command voltage signal V_{com}, the current flowing through the PMOS transistor P_4 is higher than the current flowing through the NMOS transistor N_5, resulting in that a differential current flows out of the output terminal O_1 for current equivalence. When the voltage detection signal V_{d1} (or V_{d2}) is higher than the command voltage signal V_{com}, the current flowing through the PMOS transistor P_4 is lower than the current flowing through the NMOS transistor N_5, resulting in that a differential current

sinks in the output terminal O_1 for current equivalence. Therefore, the error signal V_{e1} may be implemented by this differential current.

[0055] PMOS transistor P_5 is coupled in parallel with the PMOS transistor P_4 for serving as a parallel mirror current branch such that the current flowing through the PMOS transistor P_5 is also representative of the command voltage signal V_{com}. NMOS transistor N_6 is coupled in parallel with the NMOS transistor N_5 for serving as a parallel mirror current branch such that the current flowing through the NMOS transistor N_6 is also representative of the voltage detection signal V_{d1} (or V_{d2}).

[0056] The output terminal O_2 of the error amplifier 23 is coupled to the PMOS transistor P_5 and the NMOS transistor N_6. When the voltage detection signal V_{d1} (or V_{d2}) is lower than the command voltage signal V_{com}, the current flowing through the PMOS transistor P_5 is higher than the NMOS transistor N_6, resulting in that a differential current flows out of the output terminal O_2. When the voltage detection signal V_{d1} (or V_{d2}) is higher than the command voltage signal V_{com}, the current flowing through the PMOS transistor P_5 is lower than the NMOS transistor N_6, resulting in that a differential current sinks in the output termi-

nal O_2. Therefore, the error signal V_{e2} may be implemented by this differential current.

[0057] The brake circuit 26 includes NMOS transistors N_7 and N_8, which have drain electrodes coupled to the gate electrodes of the NMOS transistors N_1 and N_2, respectively, and have source electrodes together coupled to the ground potential. Gate electrodes of the NMOS transistors N_7 an N_8 are synchronously controlled by the brake control signal BRK. When the brake control signal BRK is at the logic high level, the NMOS transistors N_7 and N_8 are turned on, respectively connecting the gate electrodes of the NMOS transistors N_1 and N_2 in short circuit to the ground potential. As a result, the error signals V_{e1} and V_{e2} generated by the error amplifier 23 are transformed to become the brake signals having the logic high level. For more rapidly transforming the error signals V_{e1} and V_{e2} to become the brake signals having the logic high level, the brake circuit 26 is further provided with NMOS transistor N_9 which has a drain electrode coupled to the gate electrode of the NMOS transistor N_5 of the first output stage and the gate electrode of the NMOS transistor N_6 of the second output stage and has a source electrode coupled to the ground potential. A gate electrode of the NMOS

transistor N_9 is controlled by the brake control signal BRK. When the brake control signal BRK is at the logic high level, the NMOS transistor N_9 is turned on such that the gate electrodes of the NMOS transistors N_5 and N_6 are connected in short circuit to the ground potential and then immediately become nonconductive. As a result, the error signals V_{e1} and V_{e2} generated by the error amplifier 23 are rapidly transformed to become the brake signals having the logic high level.

[0058] For more clearly understanding the operations of the motor control circuit 20 according to the present invention, hereinafter are exemplarily described with reference to FIG. 4 three operational situations: (1) a constant voltage driving operation for flowing a current through the motor M from the terminal A toward the terminal B, (2) a braking operation, and (3) a constant voltage driving operation for flowing a current through the motor M from the terminal B toward the terminal A.

[0059] As shown in FIG. 4, during an operational period T_1, the state control signals S_1 and S_3 are at the logic low level, the state control signals S_2 and S_4 are at the logic high level, and the brake control signal BRK are at the logic low level. Consequently, the switching means SW_1 and the

switching unit SQ_1 are turned off, the switching means SW_2 and the switching unit SQ_2 are turned on, and the brake circuit 26 is at the disable state. Since the terminal B of the motor M has a substantially zero voltage due to the short circuit connection with the ground potential, the voltage detection signal V_{d2} is also zero. The error signal V_{e1} is a linear signal, which has a value in the linear region between the logic high level H and the logic low level L and operates the linear unit LQ_1 in the linear mode through the feedback control. The error signal V_{e2} is pulled down to the ground potential due to the conductive switching means SW_2. As a result, the voltage detection signal V_{d1} is kept substantially equal to the command voltage signal V_{com}. In other words, the voltage at the terminal A of the motor M is kept substantially proportional to the command voltage signal V_{com}. Therefore, when the command voltage signal V_{com} is a constant, the motor control circuit 20 according to the present invention effectively achieves the constant voltage driving operation for flowing the current through the motor M from the terminal A toward the terminal B.

[0060] During an operational period T_2, the state control signals S_1 to S_4 are at the logic low level and the brake control

signal BRK is at the logic high level. Consequently, the switching means SW_1 and SW_2 and the switching units SQ_1 and SQ_2 are turned off. The brake circuit 26 transforms the error signals V_{e1} and V_{e2} to become the brake signals having the logic high level H. The brake signals V_{e1} and V_{e2} having the logic high level H simultaneously operate the linear units LQ_1 and LQ_2 in the linear mode. Therefore, the motor control circuit 20 according to the present invention effectively achieves the braking operation. Incidentally speaking, the terminals A and B of the motor M at this moment have a voltage substantially equal to the supply voltage source V_m, so the voltage detection signals V_{d1} and V_{d2} are $R_3/(R_1+R_3)*V_m$ and $R_4/(R_2+R_4)*V_m$, respectively.

[0061] During an operational period T_3, the state control signals S_1 and S_3 are at the logic high level, the state control signals S_2 and S_4 are at the logic low level, and the brake control signal BRK is at the logic low level. Consequently, the switching means SW_1 and the switching unit SQ_1 are turned on, the switching means SW_2 and the switching unit SQ_2 are turned off, and the brake circuit 26 is at the disable state. Since the terminal A of the motor M has a substantially zero voltage due to the short circuit connec-

tion with the ground potential, the voltage detection signal V_{d1} is also zero. The error signal V_{e1} is pulled down to the ground potential due to the conductive switching means SW_1. The error signal V_{e2} is a linear signal, which has a value in the linear region between the logic high level H and the logic low level L and operates the linear unit LQ_2 in the linear mode through the feedback control. As a result, the voltage detection signal V_{d2} is kept substantially equal to the command voltage signal V_{com}. In other words, the voltage at the terminal B of the motor M is kept substantially proportional to the command voltage signal V_{com}. Therefore, when the command voltage signal V_{com} is a constant, the motor control circuit 20 according to the present invention effectively achieves the constant voltage driving operation for flowing the current through the motor M from the terminal B to the terminal A.

[0062] It should be noted that although in the embodiment shown in FIG. 2 the linear units LQ_1 and LQ_2 are coupled between the supply voltage source V_m and the motor M and the switching units SQ_1 and SQ_2 are coupled between the motor M and the ground potential, the present invention is not limited to this and may be applied to a case that the linear units LQ_1 and LQ_2 are coupled between the

motor M and the ground potential and the switching units SQ_1 and SQ_2 are coupled between the supply voltage source V_m and the motor M. In this case, the terminals A and B of the motor M are connected in short circuit to the supply voltage source V_m, respectively, when the switching units SQ_1 and SQ_2 are turned on. Under the feedback control, the linear units LQ_1 and LQ_2 provide the equivalent resistances between the terminals A and B of the motor M and the ground potential, respectively.

[0063] While the invention has been described by way of examples and in terms of preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications.